APPARATUS AND METHOD FOR RESPONDING TO DATA RETENTION LOSS IN A NON-VOLATILE MEMORY UNIT USING ERROR CHECKING AND CORRECTION TECHNIQUES

Abstract of the Invention

In a non-volatile memory unit such as a flash memory unit, the degradation of charge can result in an error during a read operation. By using the error checking and correction techniques, a determination can be made whether a detected error can be corrected and, if correctable, is the consistent with charge degradation at that bit position displaying the error. When a correctable error is detected, the signal group address and the correction pattern are stored and an interrupt request flag applied to the central processing unit. When the interrupt flag is processed, the central processing unit, using the signal group address and the correction pattern, restores the charge of the bit position in the memory unit. In this manner, further read operations involving the restored bit position will not repeat the corrected error.